ABSTRACT
An improved frequency compensation technique is presented for low-power low-voltage three-stage operational amplifiers with high capacitive loads. The technique uses single RC Miller compensation and a direct gain enhanced feedforward path from the input to the output. With a load capacitance of 300 pF, the amplifier nominally achieves a dc gain of 74 dB, a 3-dB bandwidth of 2.9 kHz, a 52 degrees phase margin, and a slew rate of 0.22 V/μs, while consuming 0.24 mW of power with a 1.2-V supply voltage, in a 180nm CMOS technology. The 3-dB bandwidth is one of the highest reported for a high-gain three-stage CMOS amplifier.

Categories and Subject Descriptors
B.7 [Integrated Circuits]: Types and Design Styles – Advanced technologies.

General Terms: Design

Keywords
CMOS amplifier, transconductance amplifier, frequency compensation, miller compensation, process variations, nulling resistor.

1. INTRODUCTION
In low-voltage analog circuits, voltage swing requirements prevent the use of cascode stages to build high-gain op-amps. To obtain high gains, it is necessary to design multistage amplifiers, each of which is typically a common-source stage. Multistage amplifiers suffer from closed loop stability problems due to their multiple-pole nature, as each stage introduces an additional pole. Also, as compared to two stage amplifiers, multistage amplifiers suffer from bandwidth reduction, and high dc biasing currents (and therefore high dc power consumption) are needed to increase the bandwidth when the amplifier is driving high capacitive loads.

1.1 Literature Review
To ensure stability, enhance the gain-bandwidth product, and obtain a better transient response, various frequency compensation techniques have been proposed. The following is a brief, and necessarily incomplete, overview of the literature on frequency compensation of multistage amplifiers.

Miller compensation and RC-Miller compensation [1, 2] are standard text-book techniques used in two-stage amplifiers. For three-stage amplifiers, the following are some techniques that have been proposed in the literature: Huising [3] proposed a nested-Miller (NMC) compensation technique in which a Miller capacitor was placed between the overall output of the amplifier, and the output of each of the previous stages. For a three-stage amplifier, two capacitors are necessary, because just one capacitor does not move the first non-dominant pole far away enough from the origin to obtain a stable system. The overall bandwidth of this technique is lower than other techniques, but so is the power consumption, because there is no dc power consumed by the compensation paths. Also, since Miller capacitors cause a dominant pole at the input of the amplifying stage, the output node of the amplifier always causes a non-dominant pole. Thus for large load capacitances, effective frequency compensation requires that the Miller capacitor value be proportionately large, so that the non-dominant pole at the output falls beyond the unity-gain frequency. This results in a lower bandwidth, and large-area Miller capacitors. You, et al. [4] proposed a nested Gm-C (NGC) technique; feed-forward transconductors were placed in parallel with each Miller capacitor of the nested-Miller scheme of [3]. Each feed-forward path adds a zero to the transfer function. These zeros can be used to cancel non-dominant poles or to improve the transient responses by appropriate placement of the zeros in the complex frequency plane. The feed-forward paths add to the dc power consumption, circuit complexity, and chip area. Leung, et al. [5] proposed a damping-factor control (DFC) scheme, in which they had only one Miller capacitor, in parallel with a transconductor. The lack of a second Miller capacitor caused the two non-dominant poles to become complex, thus causing an under-damped transient response (i.e. a damping factor less than 0.707). To improve the damping factor, they introduced additional damping factor control circuitry. The overall bandwidth was better than in the nested-Miller scheme; the price to pay was additional circuit complexity. Leung and Mok [6] derived accurate stability conditions for the nested-Miller scheme (that included the effects of the zeros in the transfer function), and then proposed a modified scheme that included a (nulling) resistor in series with the Miller capacitors, along with a feedforward transconductor. The nulling resistor canceled the right-half-plane zero as in the usual RC-Miller compensation, and the feedforward path with the third amplifier stage formed a push-pull amplifier that increased the slew rate, and reduced the output impedance. Ramos and Steyaert [7] used one Miller capacitor (between the outputs of the first stage and the third stage), and another capacitor across the second stage – which had a positive voltage gain. This latter capacitor, therefore, was a positive feedback.
path, rather than a Miller capacitor. The authors showed that this capacitor led to an improved transient response; the capacitor value was small, and therefore it did not significantly affect the slew rate of the first stage either. Thandri and Silva-Martinez [8] proposed a capacitor-less compensation scheme for a two-stage amplifier, by using a feedforward transconductor that would create a zero which will cancel the first non-dominant pole. The scheme could be extended to multiple-stage amplifiers also. Lee and Mok [9] proposed an active feedback compensation (AFC) scheme in which a transconductor (gma) was placed in series with the Miller capacitor. This had two effects: First, on the input side, the Miller capacitor appeared multiplied by the transconductance (gma), so that the capacitance value, and hence its chip area, were greatly reduced; and second, due to its reduced value, the Miller capacitor reflected at the output node also had a reduced value, thus causing the non-dominant pole to be further away from the origin, and hence improving the frequency response. Chan and Chen [10] introduced a voltage amplifier in series with a feedforward transconductor (GFPC). This brought the zero produced by this path closer to the origin, which could then be used to cancel a low-frequency pole, and therefore improve the overall bandwidth. The technique is particularly useful when there are large capacitive loads, which cause a low frequency non-dominant pole at the output node, as discussed earlier. Fan, et al. [11] proposed a scheme with a single Miller capacitor, with two feedforward transconductors (SMFC), one from the input to the output of the second stage, and the other from the output of the first stage to the overall output. The first transconductor canceled the first non-dominant pole; it also added to the total transconductance at the second output node, which pushed the pole at that node to a higher frequency. The second transconductor improved the transient response of the amplifier. Peng and Sansen [12] introduced a transconductance with capacitance feedback compensation technique (TCFC) where the transconductance stage and the two capacitors introduced a negative feedback to a three-stage amplifier.

1.2 Proposed Design and Paper Organization
This paper proposes a new compensation scheme, applicable especially for large capacitive loads. The scheme is shown in Fig. 1, and is described in detail in the next section.

The final design has a high 3-dB bandwidth (2.9 kHz) and GBW product (21.9 MHz – perhaps the highest reported in a three stage CMOS amplifier design), with a 0.24 mW dc power consumption – one of the lowest reported for such an amplifier. The rest of the paper is organized as follows: The proposed design and its analysis are described in Sec. 2, followed by the CMOS implementation of the scheme. Simulation results, performance comparisons, and statistical parameter variation results are in Sec. 3, and conclusions are presented in Sec. 4.

2. PROPOSED SCHEME
In nested Miller compensation [3], the inner Miller capacitor causes the first non-dominant pole to move to lower frequencies [12], which causes the gain-bandwidth product (GBW) and phase margin to be smaller. Lee and Mok [9] replaced the inner Miller capacitor with a feedforward path in parallel with the first Miller capacitor, but this feedforward path changed the positions of the poles. In the proposed scheme, single RC-Miller and gain-enhanced feedforward-path compensation (SMGFC), shown in Fig. 1, are used. The gain-enhanced feedforward path is connected directly between the input and output of the amplifier. The Miller path creates the dominant pole at the output node of the first stage. The first non-dominant pole occurs at the output node for large capacitive loads, and is cancelled by the zero created by the $R_mC_m$ Miller path. The second non-dominant pole is cancelled by the feedforward path, where $g_{mf}$ should be large enough. Therefore, a voltage amplifier is added in the feedforward path. Hence the overall feedforward transconductance is given by $g_{mf,ff} = A_v^*g_{mf}$ [10]. This allows a smaller $g_{mf}$ value, which leads to a reduction in the overall current, and therefore power consumption. This allows the dominant pole to have a high value, while still maintaining a good phase margin, hence a good transient response. The overall area reduces due to two factors: (i) the absence of the second compensation capacitor; and (ii) the reduction of $g_{mf}$ due to the gain enhanced voltage amplifier. The dc power consumption is reduced due to two primary factors: (i) The reduction in $g_{mf}$; and (ii) the short channel length used in the design (0.18 μm), which yields a high GBW at lower currents. The repercussion of the shorter length is that the mid-band gain is lower.

2.1 Small Signal Analysis
In Fig. 1, $R_1$ and $R_2$ are the output resistances of the first and second stages, respectively. Similarly, $C_1$ and $C_2$ are the output capacitances. $R_L$ is the output resistance of the third stage and $C_L$ is the total capacitance (including the load capacitance). The following assumptions are made to simplify the small-signal analysis: (i) The load capacitance and the compensation capacitance are much greater than the internal transistor capacitances; and (ii) each stage has a gain much greater than unity. Based on these assumptions, the transfer function ($A_v(s)$) of the proposed architecture is derived, and is shown at the bottom of the next page, where $A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_L$. 

Figure 1. Proposed compensation scheme